CLAIMS

What is claimed is:

1. A method for forming shallow trench isolation structures, the method comprising:

providing a substrate having a cell region and a periphery region;

forming a hard mask upon the substrate so as to cover at least a portion of the cell region and at least a portion of the periphery region;

forming a patterned photoresist layer upon the hard mask, the photoresist layer exposing a portion of the hard mask in the cell region and exposing a portion of the hard mask in the periphery region;

performing a first etching process to remove substantially all of the hard mask layer exposed by the photoresist layer in the periphery region and to remove a portion of the hard mask layer exposed by the photoresist layer in the cell region;

performing a second etching process to partially form a trench having rounded corners in the periphery region and to remove more of the hard mask layer in the cell region;

performing a third etching process to deepen the trench formed in the periphery region while maintaining the rounded corners thereof and to form a trench in the cell region; and

filling the trench in the periphery region and filling the trench in the cell region with an insulating material.

2. The method as set forth in claim 1, further comprising removing the photoresist after performing the third etching process.

3. The method as set forth in claim 1, further comprising removing the hard mask after filling the trench with an insulating material.

4. The method as set forth in claim 1, further comprising forming a pad oxide layer upon the substrate prior to forming the hard mask thereon.

5. The method as set forth in claim 1, further comprising forming a pad oxide layer upon the substrate prior to forming the hard mask thereon and removing the pad oxide layer after filling the trenches with an insulating material.

6. The method as set forth in claim 1, wherein performing a first etching process comprises removing all of the hard mask layer exposed by the photoresist layer in the periphery region.

7. The method as set forth in claim 1, wherein performing a second etching process comprises removing substantially all of the hard mask layer exposed by the photoresist layer in the cell region.

8. The method as set forth in claim 1, wherein the hard mask layer comprises a silicon nitride layer.

9. The method as set forth in claim 1, wherein the corners of the trench formed in the cell region are not substantially rounded.

10. The method as set forth in claim 1, wherein an etching gas of the first etching process comprises one of CF_4/CH_2F_2 and CF_4/CHF_3.

11. The method as set forth in claim 1, wherein an etching gas of the second etching process comprises CF_4/CHF_3.

12. The method as set forth in claim 1, wherein an etching gas of the third etching process comprises Cl_2/O_2.

13. The method as set forth in claim 1, wherein filling the trench in the periphery region and filling the trench in the cell region comprise filling the trench in the periphery region and the trench in the cell region with the same material.

14. The method as set forth in claim 1, wherein filling the trench in the periphery region and filling the trench in the cell region comprise filling the trench in the periphery region and the trench in the cell region with an oxide during a single processing step.

15. The method as set forth in claim 1, wherein filling the trench in the periphery region and filling the trench in the cell region comprise filling the trench in the periphery region and the trench in the cell region with silicon dioxide.

16. The method as set forth in claim 1, wherein the round corners of the trench formed in the periphery region have a radius between approximately 30 nm and approximately 60 nm.

17. The method as set forth in claim 1, wherein the round corners of the trench formed in the periphery region have a radius of about 60 nm.

18. The method as set forth in claim 1, wherein the trench in the periphery region and the trench in the cell region are formed so as to have approximately the same depth.

19. A method for forming trenches for shallow trench isolation structures, the method comprising:

etching a hard mask of a periphery region deeper than a hard mask of a cell region during a first etching process;

etching the hard mask of the cell region further and etching the substrate of the periphery region so as to partially form a trench having rounded corners during a second etching process; and

etching the substrate in the cell region so as to form a trench in the cell region and etching the substrate in the periphery region so as to deepen the trench formed therein during a third etching process.

20. A shallow trench isolation structure formed using a process as set forth in claim 19

21. A method for forming trenches for shallow trench isolation structures, the method comprising:

etching a hard mask of a periphery region approximately down to a pad oxide layer and etching a hard mask of a cell region less than down to a pad oxide layer so as to leave a remaining portion of the exposed hard mask of the cell region during a first etching process;

etching the remaining portion of the exposed hard mask of the cell region approximately down to the pad oxide layer and etching the substrate of the periphery region so as to form a trench having rounded corners during a second etching process; and

etching the substrate in the cell region so as to form a trench therein and etching the substrate in the periphery region so as to deepen the trench formed therein during a third etching process.

22. A shallow trench isolation structure formed by a process as set forth in claim 21.

23. An integrated circuit having shallow trench isolation structures within a substrate, the shallow trench isolation structures being formed by a process as set forth in claim 21.

24. Shallow trench isolation structures comprising:

a first trench formed in a peripheral region of a substrate, the first trench having rounded corners; and

a second trench formed in a cell region of a substrate, the second trench having unrounded corners.

25. An integrated circuit comprising:

a substrate having a peripheral region and a cell region;

a first trench formed in the peripheral region of the substrate, the first trench having rounded corners; and

a second trench formed in the cell region of a substrate, the second trench having unrounded corners.